**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

**LISTING OF CLAIMS:**

Claims 1 to 14 (Canceled)

15. (Previously Presented) A method for loading input data into a program when performing a cash transaction authentication between and electronic cash chip card and a security module, the chip card including a stored credit balance, the method comprising:

debiting a requested cash amount from the chip card using a security function;

adding and storing the requested cash amount in a cash amount summing counter of the security module,

subdividing the input data into a plurality of data blocks;

loading the plurality of data blocks into a linear-feedback shift register for performing the program, the linear-feedback shift register having at least one non-linear function cryptographically enhanced using at least one downstream counter;

introducing at least one additional feedback into the linear-feedback shift register following the at least one downstream counter; and

switching off the at least one additional feedback after a predefined first number of pulses of an associated clock.

16. (Previously Presented) The method as recited in claim 15 wherein the input data includes at least a random number, a secret key, and non-secret chip card data.

17. (Previously Presented) The method as recited in claim 15 wherein the input data includes at least a random number, a secret key, and non-secret chip card data, the secret key being associated with the non-secret chip card data, the input data being subdivided so that the non-secret chip card data and the secret key form a first data block and the random number forms a second data block.

18. (Previously Presented) The method as recited in claim 15 further comprising calculating

an authentication token, wherein a different contents of the at least one downstream counter are used during the loading step than are used after the loading step in the calculating the authentication token.

19. (Previously Presented) The method as recited in claim 15 wherein a first downstream counter of the at least one downstream counter counts to 1.

20. (Previously Presented) The method as recited in claim 15 further comprising calculating an authentication token, wherein the at least one downstream counter and the first number of clock pulses are selected so as to enable the calculating of the authentication token to be based on a second number of clock pulses.

21. (Previously Presented) The method as recited in claim 15 further comprising outputting bits after the loading is completed.

22. (Previously Presented) The method as recited in claim 15 wherein the linear-feedback shift register forms at least part of a circuit, and further comprising:

outputting bits after the loading of the blocks is completed; and

pulsing the circuit for a third number of pulses of the clock while maintaining the at least one additional feedback between the loading of the blocks and the outputting of the bits.

23. (Currently Amended) The method as recited in claim 15 wherein the linear-feedback shift register forms at least part of a circuit, and further comprising:

outputting bits after the loading of the blocks is completed;

switching off the at least one additional feedback; and

pulsing the circuit for a third number of pulses of the clock after the switching off of the at least one additional feedback.

24. (Previously Presented) A device for loading input data into a program when performing an authentication using a cryptographic MAC function, the device comprising:

a first counter;

a linear-feedback shift register having a nonlinear feed-forward function for reading off from the linear-feedback shift register, and for influencing an output of the linear feedback

shift register using the first counter, the linear-feedback shift register forming at least part of a circuit;

at least one second counter for performing the program, the at least one second counter connected downstream of the linear-feedback shift register; and

at least one additional non-linear feedback shift register for cryptographically enhancing the circuit and being connected to the circuit, the at least one additional nonlinear feedback shift register being disconnectable.

25. (Previously Presented) The device as recited in claim 24 further comprising a latch, and wherein an additional feedback is tapped off following a first of the at least one second downstream counter and before the latch.

26. (Previously Presented) The device as recited in claim 24 further comprising a latch, and wherein an additional feedback is read off from the latch following a first of the at least one second downstream counter.

27. (Previously Presented) The device as recited in claim 24 wherein an additional feedback is read off following a second of the at least one second downstream counter.

28. (Previously Presented) The device as recited in claim 24 further comprising a latch, and wherein an additional feedback is generated as an XOR sum of readouts following a first of the at least one second downstream counter before the latch, from the latch following the first of the at least one second downstream counter, and following a second of the at least one second downstream counter.

29. (Previously Presented) The device as recited in claim 24 wherein the first counter and the at least one second counter are subdivided or reduced.